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A Survey of Modelling and Circuit Synthesis for independently controlled double gate Finfet Devices

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Abstract

As compared to bulk CMOS the Double-Gate Transistors have emerged as favourable devices for nano-scale circuits because of their better scalability. The independently controlled both the gates of transistor can be used to combine parallel transistors without driving in critical paths. This can be done by independently controlling back & front gates in Double Gate Transistor. This results in reduce of switching capacitance. Hence the power dissipation of the circuit is also reduced. In this paper we tried to analyze circuit synthesis for the DG FinFET Devices. We analyze different circuits that can be advanced by using DG Transistors e.g. Schmitt triggers, SRAM cells etc. In this paper we show the advantages of 4T FinFET over conventional 3-T FinFET, which has a good potential for area efficient low power circuit designing.

Index Terms: *CMOS, Transistor, Circuit etc*

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1. INTRODUCTION

Bulk CMOS technology is currently going through certain problems such as increased leakage and process variations along with shrinking of devices dimensions. This problems faced while using CMOS technology has motivated researchers to go for non-classical silicon devices to extend scaling of CMOS more than 45nm mode. According, to the recent studies double gate devices are best replaceable devices of CMOS. Quasi-planar FinFet among various DG devices is simple to manufacture than that of planar double gate devices. FinFet consists of very thin undopped body to compress subsurface leakage paths, and it reduces short channel effect. This kind of doping solves the threshold voltage phenomenon due to random fluctuations of dopant and it increases transport of carrier which leads to higher current.

FinFET on the basis of gate connection is classified into two categories –

1. 3-T Fin-FET: FinFet connecting together front gate and back gates in a three terminal device. Bulk CMOS devices in the standard CMOS circuit design can be replaced by 3-T FinFet device.

2. 4T FinFet: This FinFet is a four terminal devices due to isolate gate and separate gate contacts. One can select to connect back and front gate together or can even connect them separately. 4T FinFet has many more options of design as shown in figure. One can have all gates like 4T or can choose to have3T FinFet or 4T FinFet accordingly. According to the selection of 4T FinFet one can have different circuit design. For example, the gate at the back can be connected to the ground in order to save switching power. 4T FinFet devices can also merge parallel transistors in the non-

critical paths to reduce power dissipation. The phenomenon of selective use of 4T FinFet devices in circuits is known as independently controlled DG FinFet technology.

Recently, performance have been demonstrated using it in IG FinFet technology for various small scale circuits like Schmitt Trigger, memory, and individual logic gates such as NAND/NOR.

In this paper we will put lights on the following topics:

1. Several low power IG logic gate options consisting of one or more 4T FinFET.
2. Semi analytical models to compare delay and short circuit power for different 3-T as well as IG FinFet logic cells.
3. FinFet-design-library-based circuit with framer-work to get efficient low-power circuit design in IG technology.

II. Double Gate SOI devices

For replacement of conventional single gate bulk CMOS devices, both the gates of Double Gate (DG) are connected together which results in a 3-T device. These typical DG devices are referred to as Independent Gate (IG) devices. The IG devices with a secondary gate for each of the devices are referred to as 4-T terminal devices. In these type of technologies, one can choose his own to connect both the front and back gates together or separately while designing a new circuit accordingly. To save switching power and areas in circuit faster paths are downsized usually. Gate size is quantized to number of fins (n_{Fin}). Each Fin has 2 conducting channels on either side. Thus a sizing step in FinFET technology is equivalent to sum a single fin, corresponding to minimum discrete sizing step as

$$\Delta W = W_{Fin} = 2H_{Fin} \quad (1)$$

H_{Fin} here indicates fin height, which is commonly also termed as width quantization. The advantage of using 4T over 3T is it offers minimum gate size $W_{min} = H_{Fin}$, i.e. half that of in 3T devices

Background Information

Figure shows circuit having critical path consisting of 3 logic gate delays. Assuming the FinFET design of the circuit, we can see that 3T have smaller gate delays because of higher I_{ON} and it can also be used in critical paths. However the remaining path shown is the non-critical path of the circuit. The dashed line shown in figure is thus non-critical path and it can be downsized also. This kind of skewed IG FinFETs can be used in the non-critical paths in the purpose of reducing dynamic power dissipation. The lower leakage current is one of the major advantages of DG transistors. Back gate bias can also be used to dynamically adjust the threshold voltage of front gate to tune power and high performance requirement of a circuit. This can also be used to merge parallel transistors or we can use in driving non-critical transistors in a single gate driven mode for reducing power.

III. Current model for FinFET Devices

We use the n^{th} power law to compute the current in FinFET. This current model is easy extraction of model parameters from a set of I_{DS}–V_{DS} characteristics (generated from simulator)

$$I_D = \frac{W_{eff}}{L_{eff}} B(V_{GS} - V_{th})^n$$

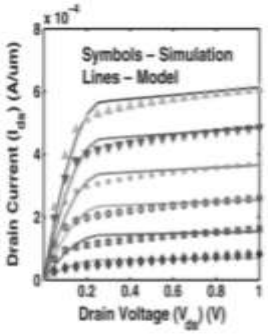
$$\text{where} \begin{cases} V_{Dsat} = K(V_{GS} - V_{th})^m \\ V_{DS} \geq V_{Dsat} : \text{saturated region} \end{cases}$$

$$I_D = I_{Dsat}\left(2 - \frac{V_{DS}}{V_{Dsat}}\right)\frac{V_{DS}}{V_{DSAT}}$$

$$\text{when } V_{DS} < V_{Dsat} : \text{linear region}$$

$$I_D = 0, \quad \text{when } V_{GS} < V_{th} : \text{cutoff region}$$

Here, W_{eff} and L_{eff} are effective channel width and channel length. V_{th} is the transistor threshold voltage, I_D is drain current. Here, n, m, K and B are constants to describe SCEs. From a few TAURUS simulated I_{DS}–V_{DS} characteristics shown in the figure, we extract the value of these constants for both 3-T and 4-T devices. These current models are then used to predict the I_{DS}–V_{DS} characteristics of the 3-T and 4-T devices with various number of fins. Fig. 6 shows close match of the predicted current in4-T FinFET with simulation results that are obtained from simulator, in the saturation mode. Slight deviation in the linear mode i.e. low V_{DS} region has negligible impact in rise or fall delay and transition time estimation.



IV. Delay, Area and Power of 4-T FinFET-Based Circuits

While introducing 4-T FinFET in circuit, it has two implications on its overall performance. We explain these with reference to IG NAND gate, as shown in Fig.

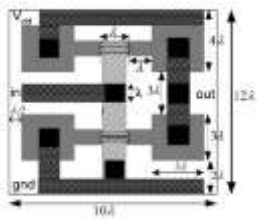


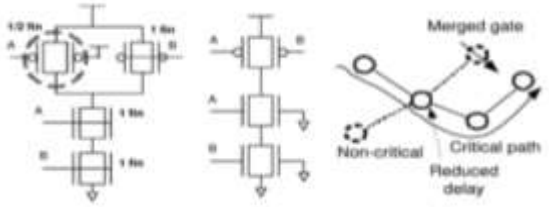
TABLE I

Gate name	Input drive ΣW_{Fin}	Input cap ΣC_{gate}	A_{saving} (%)	C_{sw} saving (%)
NOR2 (3-T)	3	10	0	0
IG NOR2	4.5	9	-7	10
MG NOR2	2.5	5	28.7	50
MG×1 NOR2	1.5	3	28.7	70
MG×2 NOR2	3	5	28.7	50
NAND2 (3-T)	2	4	0	0
IG NAND2	3.5	5	-7.1	25
MG NAND2	1	2	14.3	50
INV (3-T)	1	6	0	0
IG INV	1.5	3	-9.1	50
IGx INV	1	2	-18.2	67

1. The loading of gate driving node "A" reduces and thus its input arrival time reduces.

However, charging current due to switching at input "A" reduces 50% more in independent gate mode. Due to the corresponding input transition output signal transition time is increased. For rising output transition, because of these two opposing effects, the effective increase in delay of the noncritical node is 50% less than of the conventional 3-T FinFET-based circuit. However, loading of previous stage reduces by 25%, improving its delay [Fig. 2(a)]. Under certain situations, one can get an improvement in the critical path delay due to the reduced switching capacitance in critical path fan-out shown in figure [Fig. 2(c)]. In figure merging of two parallel 3-T devices in the MG-Cell, lying in the off-critical path, effectively reduces capacitive loading of the cell driving the MG-Cell. If the previous stage cell is in the fan-out logic cone of a critical node, the corresponding critical path delay reduces. This can potentially improve the overall circuit delay and/or robustness due to reduction in the number of critical paths. Both the IG- and MG-Cell options of FinFET have reduced switching capacitance, resulting in significant power savings. For a two-input merged NAND gate, we save about 50% switching capacitance (Table I), if compared to minimum-sized conventional 3-T FinFET-based NAND gates. Similarly exploring the noncritical path of NOR cell, we get two different versions of independently controlled NOR cell, as showninFig.3(a)and(b).It is important to note one can obtain balanced rise and fall delays with the merged cells, as shown in Figs. 2(b) and 3(b). For balanced rise/fall transitions, NOR gate cells has higher Wp/Wn ratio compared to NAND. This results in more switching capacitance saving up to 80%, as presented in Table I below. If asymmetry is allowed in the rise and fall delays, we can have two more IG options (MG×1 and MG×2) for NOR cells and one more for INV (IG×), as shown in Fig. 4. In Fig. 4(a) and (b), the TpdLH is almost 2×and 4×of TpdHL. For more accurate estimation the impact of IG FinFET technology on the design area, we need to consider the effect of using 4-T FinFETs on the area of different logic cells. We perform cell layout based on a set of FinFET layout rules [4]. We also consider the back gate contact overhead in the IG FinFET cell considering the estimation of the cell layout area. Fig. 5 shows layout of an IG inverter corresponding to the independent gate inverter as shown in Fig. 3(c). We express the cell layout area in terms of λ, the minimum spacing requirement, as shown in Fig. 5 [4]. In case of a conventional 3-T FinFET inverter, the ground line can be moved up by λ, as it does not require a poly to metal via contact. Therefore, in IG inverter, cell footprint area increases to 120λ2 from the original 3-T area of = 110λ2. This shows 9.1% area penalty for adding an extra back gate contact to the nMOS (Table I). Similar area overhead can be observed in both the NAND and NOR IG-Cell (Table I). In merged cells, the number of transistors reduces as compared to the corresponding 3-T FinFET cell. Hence, the cell area also reduces. In NAND MG-Cell, we get about 14% area savings. However, because of higher Wp/Wn ratio of NOR logic cells, we can save 27% area for NOR MG-Cell. The relative area and switching capacitance speed (Csw) savings

of different 4T gates over their 3T counterpart are tabulated in Table I below. In the table, the second column represents the input drive in terms of number of fins connected per input. The third column represents the capacitive loading for each input.



V. DELAY MODEL FOR FINFET BASED INVERTERS

Consider a falling output transition of an inverter with a rising input ramp V_{in}, having slope S, as shown in Fig. 7. At t =0, Vin =0, Vout = Vdd. At this time, the total charge at the output node Qout can be expressed as

$$Q_{out} = Q_M + Q_L = (C_M + C_L)\, V_{LL} \qquad (5)$$

Here C_M is the effective Miller capacitance. C_M consists of gate-to-drain or source overlapping capacitance along with other parasitic components. After a small time t = dt assuming $V_{out} = V_o$

$$V_{in}=V_i(t)= \begin{cases} S\,dt = \left(Vdd\frac{}{tin}\right)dt, & dt \le tin \\ Vdd, & dt > tin \end{cases} \qquad (6)$$

Here t_{in} is the input ramp transition time. We note that, at t = dt, some charge (for example, $Q_{current}$) is being removed from the output node due to nMOS and pMOS currents I_n and I_p, respectively. At t = dt using the conservation of charge at the output node of the inverter, we have

$$Q_{out} = Q_M + Q_L + Q_{current} \qquad (7)$$

$$= (C_M + C_L)\, V_O - C_M\, V_i + dt \qquad (8)$$

Equating Q_{out} from (5) and (8) and solving for V_o,

$$V_O = V_{dd} + dt \qquad (9)$$

Hence, using (2)–(9), Vo (t = dt) can be expressed as

$$V_O = f\ (t_{in}, C_L, C_M, W_{eff}, I_p, I_n, dt) \quad (10)$$

We use numerical integration in MATLAB to compute $Q_{current}$. Hence, knowing the currents I_n and I_p at each simulation instant and using (10), we get an estimate of Vo, at t = dt It is important to note that CM varies with V_{in} and V_{out}. We observe that CM is inversely proportional to tin and CL, but directly proportional to Weff . Accordingly, C_M can be represented as $C_M = g\ (t_{in}, C_L, W_{eff})$.

This method can be extended to determine the complete transient response of the inverter output voltage. We assume that at t = To, we have an accurate estimate of output node voltage $V_O\ (T_O) = V^{old}{}_O$ using the current values of I_n and I_p (Fig. 7). By using eqn (10), we can get an initial estimate of $V_O(T_O + dt) = V^{new}{}_o$ as

$$V_O^{pred} = f\ (\ t_{in}, C_L, C_M, V^{old}{}_O, W_{eff}, I_p, I_n, T_O{+}dt) \quad (11)$$

Prediction error to estimate the $V^{new}{}_o$ at $t = T_O + dt$ is

$$\Delta Vo = V^{pred}{}_o - V^{old}{}_o \quad (12)$$

Now, we update the old estimate of $V^{old}{}_o$ as

$$V^{old}{}_1 = V^{old}{}_o +, \quad \Delta V_O > \eta \quad (13)$$

Where noIter is the number of iterations performed to get a close estimate of V new o. We then use this updated V old o to modify the values of In and Ip using (2)–(4). These modified current values help to get a closer estimate of V new o. These steps of (11)–(13) are repeated. These iterations terminate when the prediction error ΔVo goes below a small predefined threshold value η .Thus, repeatedly applying this procedure, we obtain a reasonably accurate transient response of Vout for an inverter. The parameters (noIter) η and resolution of the time step (dt) control the speed and accuracy of the inverter output transient estimation. Once the transient response is known, the propagation delays tpdLH, tpdHL can be easily extracted, as shown in Fig. 8. Fig.8 shows the excellent agreement of the proposed model's prediction of V_O with TAURUS simulator results for a 3-T inverter gate with t_{in} = 10ps and CL =1fF. As mentioned in Section III-A, the predicted transient response is slightly off from that obtained by TAURUS at the initial and final phase of the rise and fall transients. However, this has negligible impact on estimation of propagation delay (Tpd).

VII. Delay Model for 2 input logic gates

To extend the proposed FinFET inverter delayed model for multi-input NAND and NOR gates, we take the position of the switching transistor. We use the generic technique of mapping for converting any multi-input NAND/NOR gate to the equivalent inverter, as shown in [13], and new version for FinFET-based circuits. Then, we apply our proposed semi analytical delay model (Section III-B) to get the transient output voltage.

The mapping technique is to get an equivalent inverter circuit for any of the two-input logic gate with an equivalent resistance (R_{eq}) and capacitive load that is (Ceq), as shown in Fig. 9(a). This proves that both the circuits have equal first-order Elmore time constants [14]. The first-order moment of the NAND gate is

shown by

$$T_C = R_{eq}C_{eq} = (R_1 + R_2)C_0 + R_2C_1 \quad (14)$$

Since resistance is inversely proportional to the device width (W_{eff}), we should have a correct estimate of the transistor equivalent width and capacitance values to model gate delays. Note that in two-input logic, only one transistor is considered to be switching at a particular instant of time. This is a valid assumption, since in critical path evaluation, only one signal per gate is to be activated. Thus, the generic mapping problem is to simplify to find the equivalent widths for the pMOS and nMOS transistor in the form of equivalent inverter.

Modeling Equivalent Inverter Width (*W*eq)*:*

For a NAND circuit, one of the nMOS device will be in the state of conduction, and the other devices will be switched from either lower to higher (or vice versa). As a result, of the effective current driving the capability of the switching devices is only half as that of the other "on" devices. Thus, we are able to take the effective width of the switching nMOS as half of that of the other devices. Fig. 9 shows the falling output transition because of switching of the input "in 2" of a NAND circuits and its corresponding *RC* model of pull-down of network. Input "in 1" is at V_{dd}; so, the corresponding pMOS is in cutoff region and is not considered. However, this mapping concept is well fitted for bulk

CMOS circuits, which can be sized for the balanced rise and fall delays. In FinFET-based circuits, widths are integer multiples of fin height [2]. Hence, it is impossible to get the balanced rise and fall delays unless the mobility of nMOS and pMOS devices are also integer multiples of each other, which is rare case. To get

the effect of unbalanced pull-up and pull-down drive the current in FinFET-based circuits, we incorporate width correction term λ_w in the equivalent width computation as

$$W_{peq} = W_{pk}\lambda_{wp} \quad \frac{1}{W\text{neq}} = \frac{1}{\lambda\text{wn}}\left(\frac{1}{Wn2} + \frac{1}{2Wn1}\right)$$

Here, λ_{wp} and λ_{wn} are function of the mobility ratio μ_n/μ_p, gate type, and that of *t*in. However, when input "in 1" switched to low, the current path is blocked below this device [13]. Hence, lower nMOS device is in cutoff from conduction, and the equivalent inverter transistor widths are given as

$$W\text{peq} = W\text{pk}\lambda\text{wp}\ \frac{1}{W\text{neq}} = \frac{1}{\lambda\text{wn}}\left(\frac{1}{Wn1}\right)$$

2) Modeling Equivalent Capacitance (Ceq)*:*

To preserve first-order *RC* time constants of the NAND circuits during the falling transition because of switching of input "in 2," as in Fig. 9(c)

$$R_{eq}C_{eq} = \left(\frac{R1}{2} + R_2\right) C_0 + R_2C_1 \qquad (17)$$

Considering the fact that width of device is inversely proportional to resistance, (17) can be written as

$$\frac{C\text{eq}}{W\text{eq}} = \left(\frac{1}{2W1} + \frac{1}{W2}\right) C0 + \frac{1}{W2}C1 \qquad (18)$$

where *W*eq is equivalent inverter width of nMOS in (16). The capacitances *C*0 and *C*1 consists of *CL* and gate-to source/drain overlap capacitances, as depicted in the Fig. 9(b)

$$C_O = C_L + C_{on1} + C_{op1} \qquad (19)$$

$$C_1 = C_{on1} + C_{on2} \qquad (20)$$

Here C_{op} and C_{on} are the gate-to-drain or source overlap capacitances [7] of pMOS and nMOS, respectively. Hence, for the switching of input "in 2" of a NAND gate, the equivalent capacitance *C*eq can be determined as

$$C_{eq} = C_{neq} + C_{peq}, \text{ where } C_{peq} = C_{op1} \qquad (21)$$

$$C_{neq} = \left(\frac{W\text{neq}}{2W1} + \frac{W\text{neq}}{W2}\right)C0 + \frac{W\text{neq}}{W2}C1. \qquad (22)$$

Weq and C_{eq} parameters for the timing arc corresponding to input "in 1" of NAND gate can be expressed using (16)–(22).

Fig. 10 show a good match of our transient response prediction of a two-input 4-T FinFET-based NAND (IG-Cell), with TAURUS simulation results. The skewed nature (difference in TpdLH and TpdLH) of the IG FinFET cell is also evidence.

The equivalent width and capacitances for NOR can be similarly obtained by reversing the suffixes that is n- and p- in the NAND circuit equation. This mapping technique can be applied to the IG and MG FinFET cell with the corresponding I_{DS}–V_{DS} current models for 4-T FinFET device.

VIII. Simulation Results

We simulate a bunch of ISCAS85 benchmark circuits in 45-nm technology node. The following parameters are used in this paper: H_{fin} = 40 nm, T_{si} = 10 nm, and L_{eff} = 35nm.

Figure shows the increasing trend of power and area savings with target delays for an ISCAS85 benchmark circuit c880 in the IG FinFET technology over conventional 3-T FinFET design library. This is because of the fact that, at relaxed delay target, there are more opportunities for merging two 3-T devices to a 4-T FinFET device. In 3-T library-based synthesis, under certain delay constraints, a number of smaller sized (s1, s2, s3) cells are being replaced with larger sized (s2, s3, s4) cells in critical paths to meet the required timing. In extended-library based circuit design, because of the presence of smaller sized 4-T cells in the fan-out logic cone of the critical nodes, more opportunities exist to use smaller sized gates in the critical paths to meet the same performance constraint. Hence, significant area and power saving is observed in Extended library-based circuit for the reduced switching capacitance in the IG technology. In order to have a uniform delay constraint (T_{ckt}) for different circuits, we choose the individual circuit delay target as the mean of minimum and maximum circuit delay synthesizable by 3-T design library as

$$\text{Tckt} \approx \frac{(\text{TcktMin} + \text{TcktMax})}{2} \qquad (24)$$

Here, T_{cktMin} and T_{cktMax} are the fastest and slowest synthesizable delay with the conventional 3-T design in the library. Accordingly, for c880 circuit, we use Tckt = 100 ps using eqn no (24) as its delay ranges from 75 to 120 ps (Fig. 12). Fig. 13 shows power and area savings of several ISCAS85 benchmark circuits in IG FinFET design library at their corresponding mean circuit delay. On an average, across all ISCAS85 benchmarks, we have successfully obtain 18% saving in power dissipation and about 8.5% savings in design area (Fig.

13) in IG FinFET technology over the conventional 3-T FinFET-based design. As shown in the Table I, individual 4-T cell power savings are always about 2 times higher than their cell layout area savings, compared to the conventional 3-T cell. Table III lists the statistics of different types of gates in the c880 circuits synthesized using the two FinFET design libraries at two different target delay. We observe a significant reduction in minimum sized NAND/NOR gates with the extended-library-based design as they are mostly replaced by the corresponding IG-Cells. Moreover, the number of higher drive strength cells (s2, s3, s4) also reduces. In fact, because of the less capacitive loading in the fan-out logic cone of critical paths, the total number of cells reduces. Overall, we obtain significant power (22%) and area (11.6%) savings at T_D = 90 ps in IG Technology-based c880 circuit synthesis (Fig. 13).

CONCLUSION

4-T FinFET technology, with independent gate-controlled FinFET devices, has good potential for area efficient low-power circuit design. In this paper, we developed semi analytical delay and power models for IG FinFET-based logic cells, and a generic efficient design library-based circuit synthesis framework. We demonstrate that the IG FinFET-based design provides substantial power and area savings over the conventional 3-T FinFET-based design for a set of ISCAS85 benchmark circuits. Power and area savings are achieved even with a conservative worst corner-based circuit synthesis approach.

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